Wide frequency range VCO - Datasheet

Features

- Voltage-Controlled Oscillator (VCO) optimised to achieve a frequency range between 150MHz and 1.3 GHz (Fig 1)
- Linear dependency between voltage and frequency variation across 86% of the tunable range ($0.6 \leq V_{ctr} \leq 1.8$)
- Low power consumption ($P_{avg} \leq 400uW$ across all corners) and reduced area ($A = 290\mu m^2$)
- Temperature range between -150 and 50°C: frequency drift of -0.5MHz/°C (corresponding to 0.04% of the tunable range)
- High slew rate across all corners ($SR > 3V/ps$) and duty cycle of 50%
- High frequency gain ($K_{VCO} \approx 1GHz/V$); $f_{range} > 1GHz$ across all corners and mean centre frequency of $f_{osc} \approx 600MHz$ across process and mismatch, as per target specification.
- Phase Noise of -78dBc/Hz at 1MHz, with small variation of the phase performance across corners and mismatch.

General Description

This Voltage-Controlled Oscillator (Fig 2) consists of three components:

- Ring Oscillator composed by 5 current-starved inverters and two current mirrors biasing the PMOS and NMOS of the ring; the delay in the loop is proportional the size of the transistors and the amount of current provided by the mirrors; therefore, by tuning the current, the frequency will vary:

  $$f_{osc} = \frac{1}{N\tau} = \frac{I_D}{NC_{tot}AVDD}$$

  with N = number of stage, τ the delay, $C_{tot} \propto WL$ and I_D the drain current at each inverter stage.
- Input stage including an input transistor and a $10K\Omega$ poly resistor in series to convert the control voltage into a linear current biasing the current mirrors.
- Output stage consisting of 4 buffers to convert the output waveform into a rail-to-rail square wave biased at the middle of the power supply with high slew rate and 50% duty cycle.

Performance Trade-offs

The design achieves low to high frequencies maintaining a reduced area and power consumption. The frequency range and output waveform format are consistent across all corners and temperature.
The limitation of this design is an inherit trade-off between the phase noise performance and the frequency range. In the model proposed, the range has been prioritised, leading to a phase noise magnitude of around -78dBc/Hz @ 10MHz; for other applications, this design can be easily tuned to match the potential requirement of a enhanced phase stability by increasing the dimension of the inverters at the core.
Due to the small size of the components used in order to achieve high frequencies, the device has a standard deviation of the centre frequency of $\sigma = 0.150GHz$ across process and mismatch.

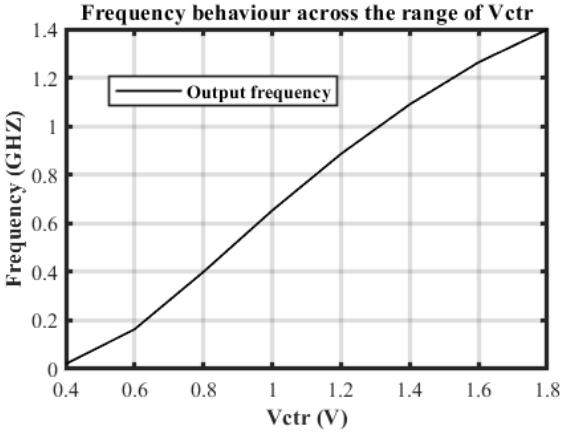


Figure 1: Complete frequency range between 20MHz and 1.4GHz, with linear behaviour across 86% of the Vctr values

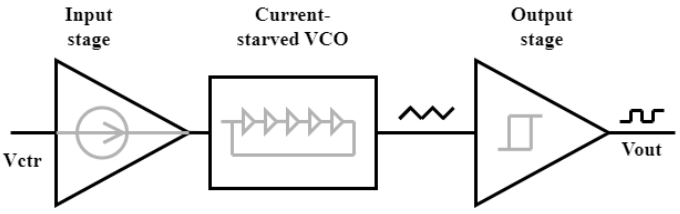


Figure 2: Circuit diagram: input stage with current linearisation, current starved ring oscillator, and output buffer with differentiation functionality

Electrical Specifications

Table 1: Electrical Specification[1]: typical values and range given by 5-Corner analysis; mean and standard deviation computed using MonteCarlo analysis across process and mismatch

Parameter	Symbol	Min.	Typ.	Max.	Mean	Std Dev.	Unit
Frequency Range	f_{range}	1.088	1.161	1.365	0.980	0.470	
Frequency Min	f_{min}	0.109	0.152	0.221	0.156	0.021	GHz
Frequency Max	f_{max}	1.197	1.313	1.586	1.135	0.449	
Frequency Gain	K_{VCO}	806.5	981.4	981.4	774.9	279.9	MHz/V
Linear Range	V_{linear}	0.6	-	1.8	-	-	V
Frequency Drift ($-50°\leq T \leq 150°$C)	F_θ	-	-0.5	-	-	-	MHz/°C
Phase Noise @ 10MHz	$S_\phi(f)^{10MHz}$	-105.60	-105.00	-104.30	-103.5	23.53	
Phase Noise @ 1MHz	$S_\phi(f)^{1MHz}$	-78.61	-77.78	-76.53	-76.98	13.05	dBc/Hz
Phase Noise @ 10KHz	$S_\phi(f)^{10KHz}$	-18.72	-17.80	-16.32	-17.97	2.174	
Harmonic 1	H_1	-	1.14	-	-	-	
Harmonic 2	H_2	-	0.36	-	-	-	V
Harmonic 3	H_3	-	0.20	-	-	-	
Supply current	I_{supply}	128.3	159.6	222.5	162.2	10.07	uA
Average Power Consumption	P_{avg}	230.9	287.2	400.6	292	18.12	uW
Slew Rate	SR	3.16	3.60	4.13	-	-	V/ps
Output Amplitude	V_{pp}	-	1.8	-	-	-	V
Duty cycle	D	50.26	50.91	51.32	-	-	V
Area	A	-	290	-	-	-	μm^2
Number of PDK components	n	-	35	-	-	-	

[1] Based on characterization data, not tested in production.

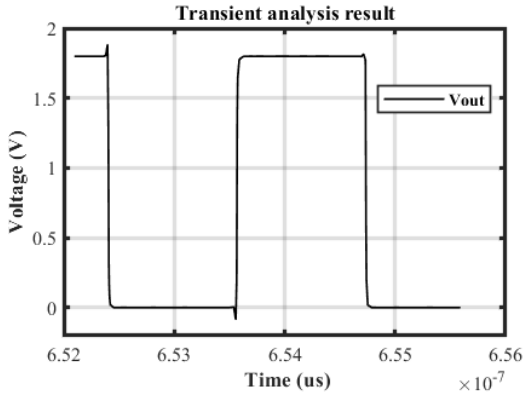
Absolute Maximum Ratings

Parameter	Rating
AVSS to AVDD	1.8 V
Vctr	0.4 to 1.8
Temperature range	-50 to +150°C

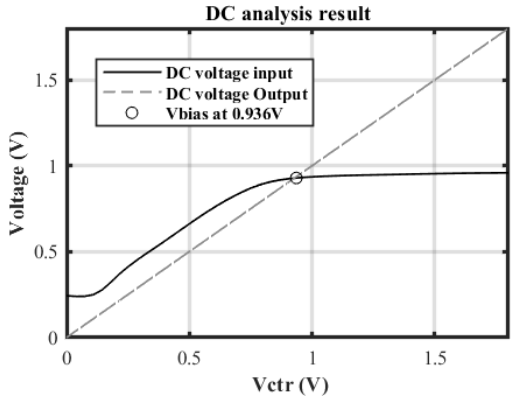
[2] Stresses above those listed under Absolute Maximum Ratings can cause permanent damage to the device. This is a stress rating only. Functional operation of the device is not implied in any conditions above those indicated in the Electrical Specifications section.

Performance evaluation

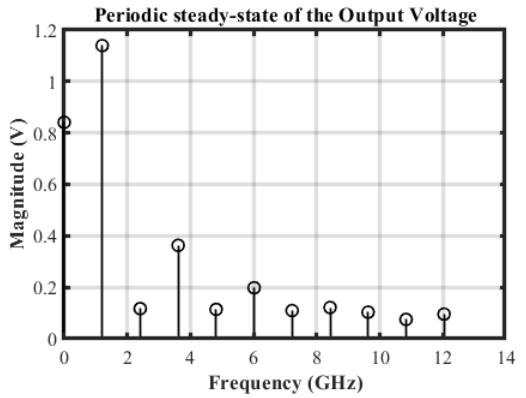
Plots (a) to (e) report the performance of the design proposed in this datasheet.
Plot (f) shows the impact of parameter tuning on the frequency behaviour, comparing possible design modalities which would focus alternatively on lower phase noise, or greater frequency range and linearity; the key parameters are the length of the inverter's transistors ($f_{range} \propto PN \propto \frac{1}{L_{inv}}$), the size of the input resistor ($R \propto$linear behaviour) and the width ration of the current mirror's transistors ($W_{cm} \propto f_{range}$)



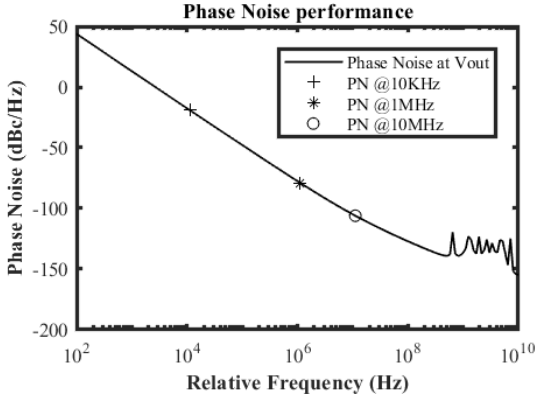
(a) Transient output waveform; $D \simeq 50\%$**;** $Vpp = 1.8V$**;** $SR = 3.6V/ps$



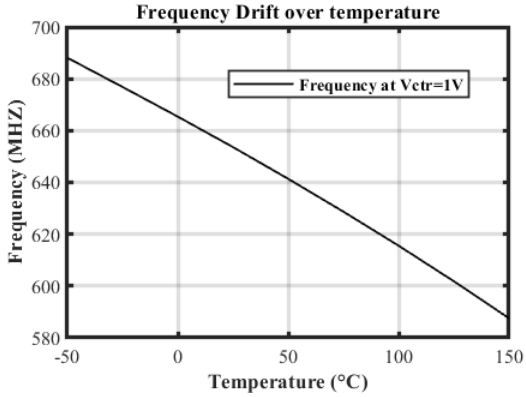
(b) Vout DC, sweeping Vin across the control range. $V_{bias} = 0.936V \simeq \frac{AVDD-AVSS}{2}$



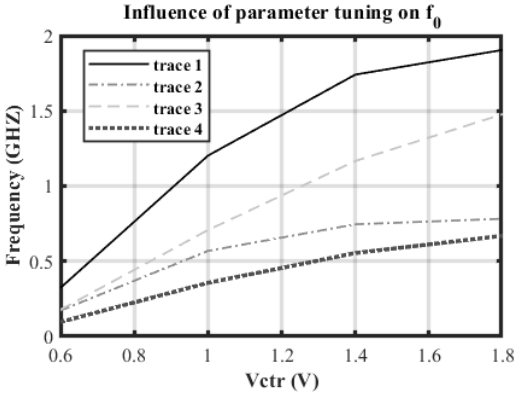
(c) Frequency spectrum of the periodic steady-state; H_1 **at 1.2GHz,** H_2 **at 2.4GHz**



(d) Phase noise analysis: Phase Noise @ 10MHz = -105.00 dBc/Hz; Phase Noise @ 1MHz = -77.78 dBc/Hz; Phase Noise @ 10KHz = -17.80 dBc/Hz.



(e) Temperature performance at $V_{ctr} = 1V$**: frequency drift of -0.5MHz/°C**



(f) Effect of tuning on the frequency range;
trace 1: $L_{inv} = 300nm$,$R = 0\Omega$, $W_{cm} = 500nm$;
trace 2: $L_{inv} = 600nm$,$R = 0\Omega$, $W_{cm} = 500nm$;
trace 3: $L_{inv} = 300nm$,$R = 10K\Omega$, $W_{cm} = 1\mu m$;
trace 4: $L_{inv} = 600nm$,$R = 10K\Omega$, $W_{cm} = 1\mu m$.

Schematic

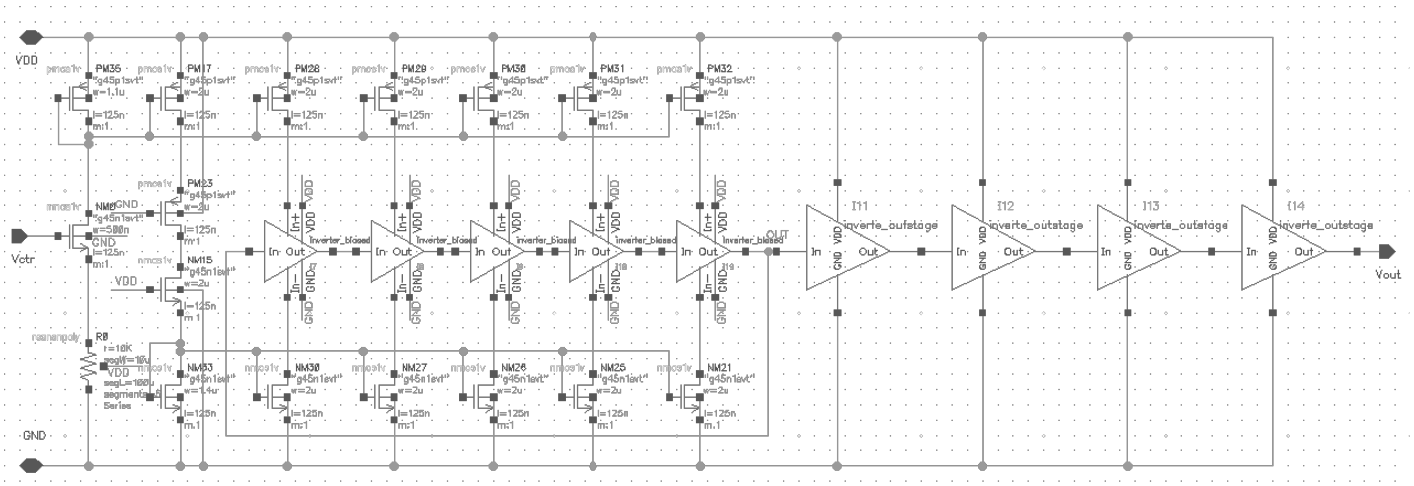
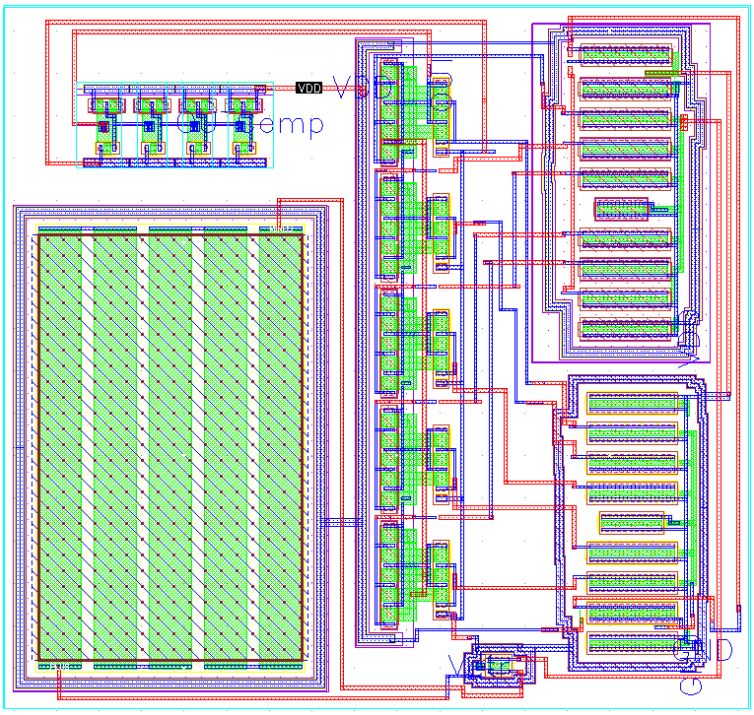


Figure 4: Full schematic of the 5-stages current-starved VCO, current linearisation at the input stage, and 4-buffer output stage (dummies excluded).

Layout




```
Host is
cmd  is /usr/local/cadence/ASSURA_04.16.109_618/tools.lnx86/assura/bin/assura /home/mp2419/nfshome/CadenceLab/
VCO_blocks.rsf -cdslib /home/mp2419/nfshome/CadenceLab/cds.lib -restart -gui
Starting the Assura DRC Run: IPC Id ipc:15: pid 7069.
Checking out license for "Assura_UI"
Checking out license for "Phys_Ver_Sys_Results_Mgr"
*WARNING* No DRC errors found.
```

```
*INFO*: Schematic integrity check is completed.
Assura LVS: State saved "Last"
Host is
cmd  is /usr/local/cadence/ASSURA_04.16.109_618/tools.lnx86/assura/bin/assura /home/mp2419/nfshome/CadenceLab/
VCO_blocks.rsf -cdslib /home/mp2419/nfshome/CadenceLab/cds.lib -gui
Starting the Assura LVS Run: IPC Id ipc:16: pid 10780.
STATUS: Schematic and Layout Match
```

Figure 5: Final layout with dummies designed to maximise symmetry and compactness, using common-centroid configuration for the current mirrors and symmetry with the inverters; proof of DRC and LVS passing is also presented